

SN54165, SN54LS165A, SN74165, SN74LS165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

The SN54165 and SN74165 devices are obsolete and are no longer supplied.

SDLS062D – OCTOBER 1976 – REVISED FEBRUARY 2002

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

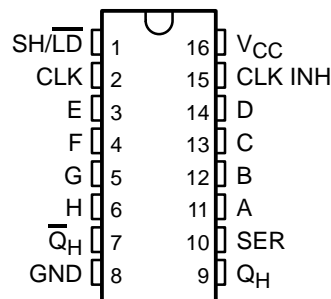
| TYPE | TYPICAL MAXIMUM CLOCK FREQUENCY | TYPICAL POWER DISSIPATION |
|---------|------------------------------------|------------------------------|
| '165 | 26 MHz | 210 mW |
| 'LS165A | 35 MHz | 90 mW |

description

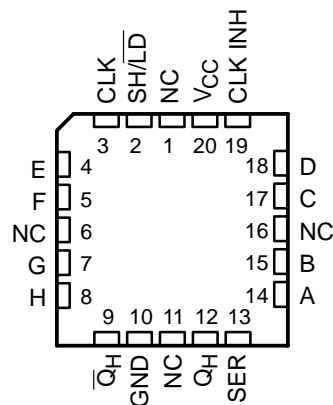
The '165 and 'LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual, direct data inputs that are enabled by a low level at the shift/load (SH/\overline{LD}) input. These registers also feature gated clock (CLK) inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a two-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with SH/\overline{LD} high enables the other clock input. Clock inhibit (CLK INH) should be changed to the high level only while CLK is high. Parallel loading is inhibited as long as SH/\overline{LD} is high. Data at the parallel inputs are loaded directly into the register while SH/\overline{LD} is low, independently of the levels of CLK, CLK INH, or serial (SER) inputs.

SN54165, SN54LS165A . . . J OR W PACKAGE
SN74165 . . . N PACKAGE
SN74LS165A . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54LS165A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74LS165AN | SN74LS165AN |
| | SOIC – D | Tube | SN74LS165AD | LS165A |
| | | Tape and reel | SN74LS165ADR | |
| | SOP – NS | Tape and reel | SN74LS165ANSR | 74LS165A |
| –55°C to 125°C | CDIP – J | Tube | SN54LS165AJ | SN54LS165AJ |
| | | Tube | SNJ54LS165AJ | SNJ54LS165AJ |
| | CFP – W | Tube | SNJ54LS165AW | SNJ54LS165AW |
| | LCCC – FK | Tube | SNJ54LS165AFK | SNJ54LS165AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

| INPUTS | | | | | INTERNAL OUTPUTS | | OUTPUT Q _H |
|----------------------------|---------|-----|-----|--------------------|-------------------------|-------------------------|-----------------------|
| SH/ $\overline{\text{LD}}$ | CLK INH | CLK | SER | PARALLEL A . . . H | $\overline{\text{Q}}_A$ | $\overline{\text{Q}}_B$ | |
| L | X | X | X | a . . . h | a | b | h |
| H | L | L | X | X | Q _{A0} | Q _{B0} | Q _{H0} |
| H | L | ↑ | H | X | H | Q _{An} | Q _{Gn} |
| H | L | ↑ | L | X | L | Q _{An} | Q _{Gn} |
| H | H | X | X | X | Q _{A0} | Q _{B0} | Q _{H0} |



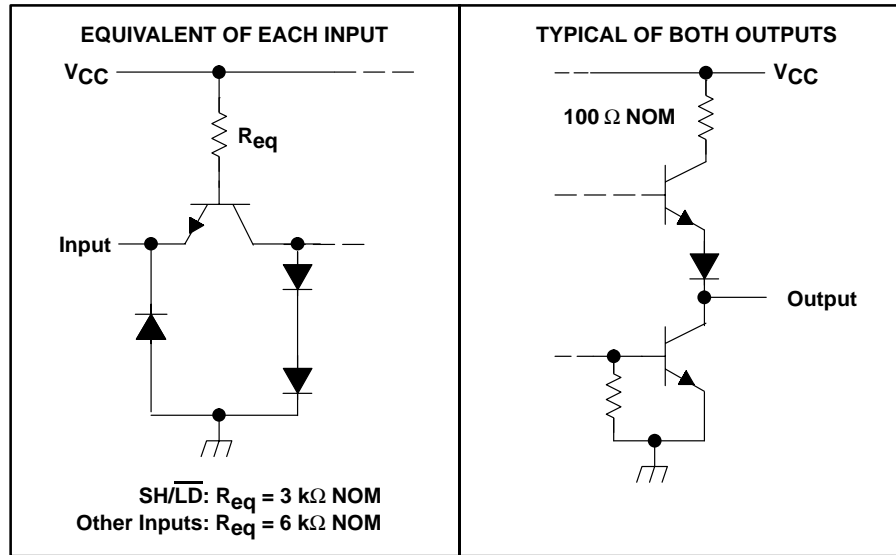
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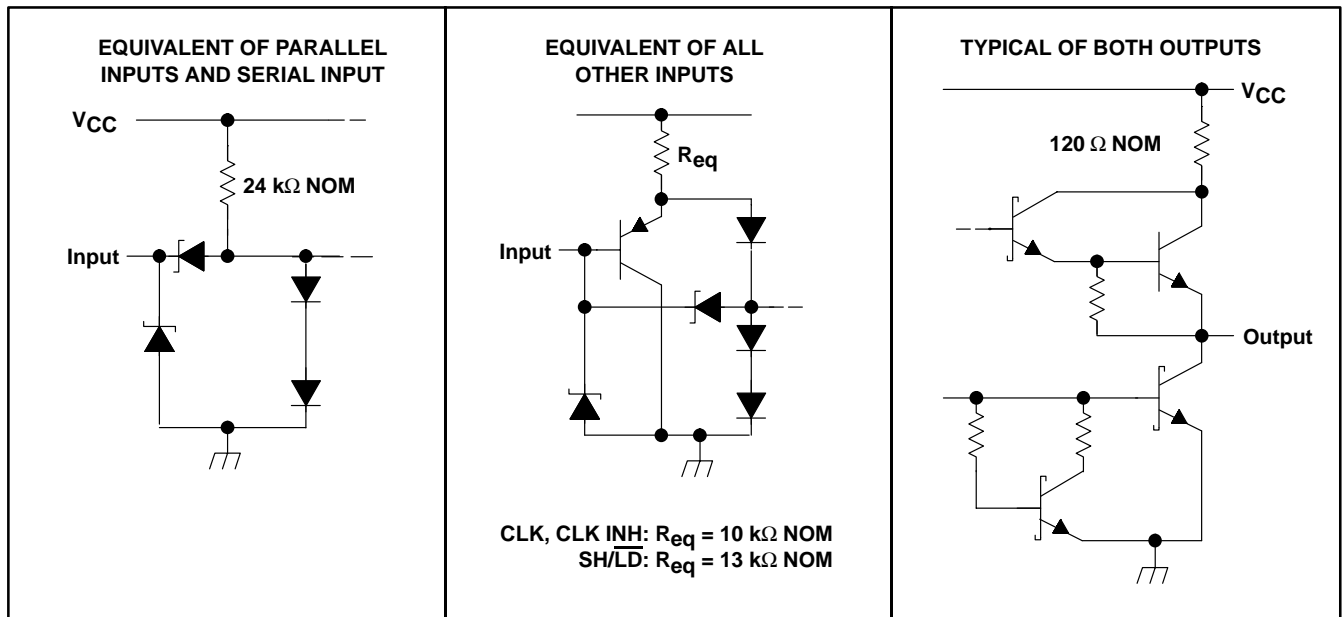
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schematics of inputs and outputs

'165



'LS165A

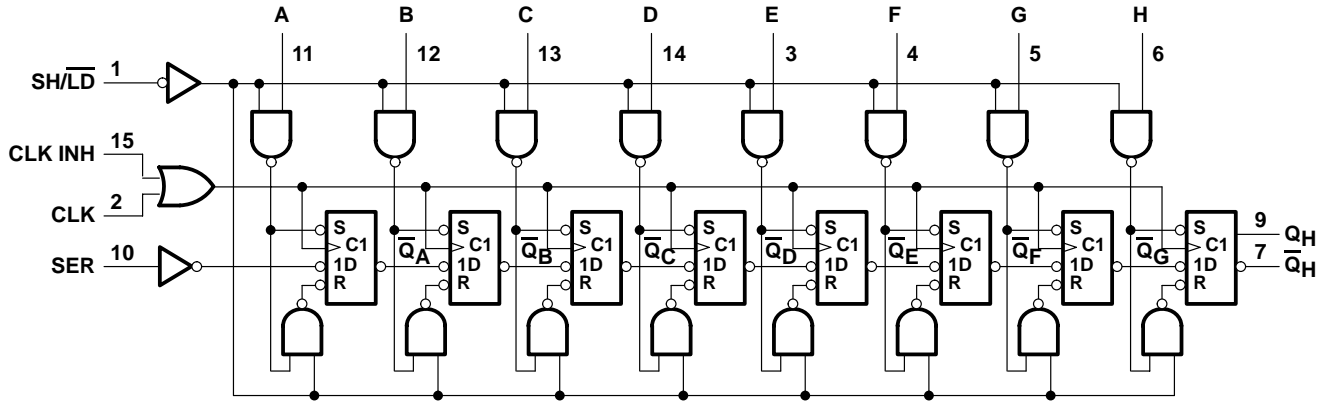


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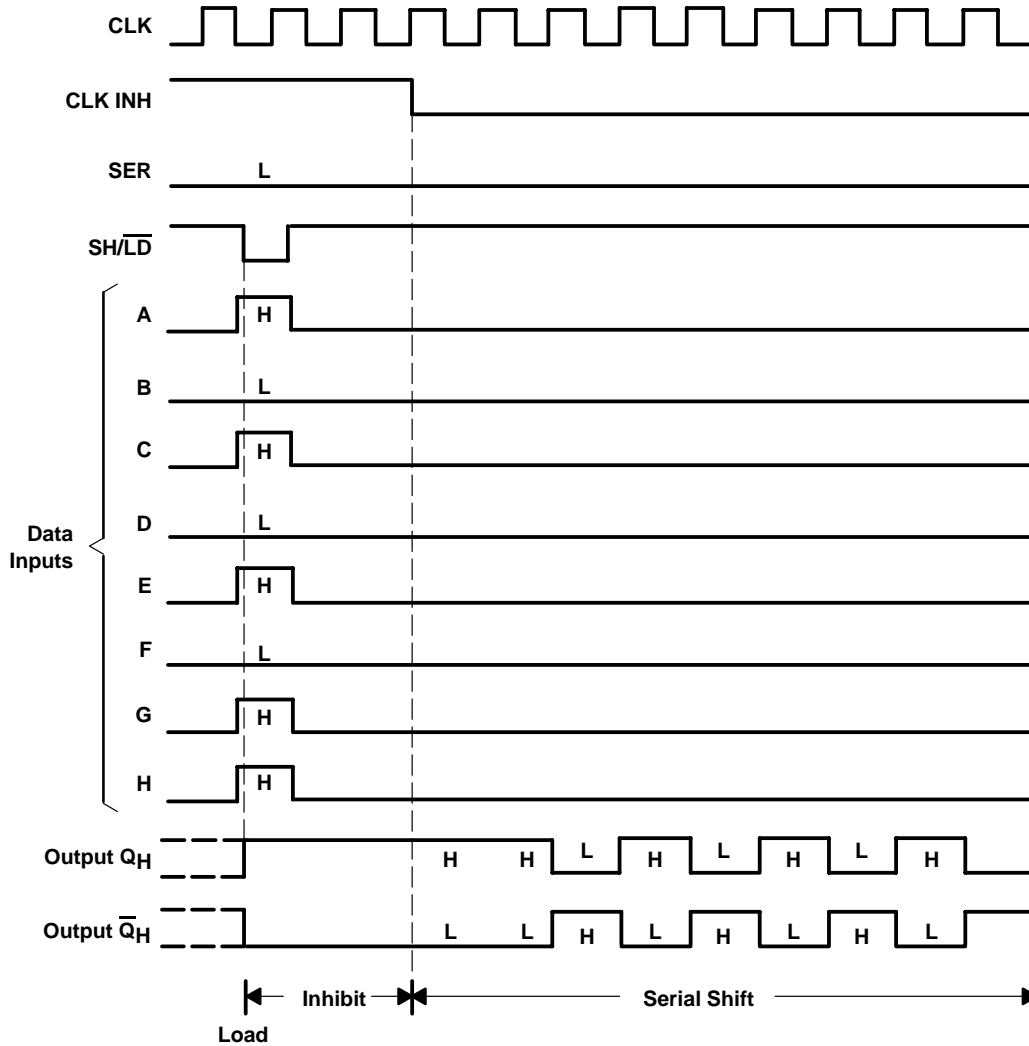
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logic diagram (positive logic)



Pin numbers shown are for D, J, N, NS, and W packages.

typical shift, load, and inhibit sequences



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I : SN54165, SN74165 | 5.5 V |
| SN54LS165A, SN74LS165A | 7 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Package thermal impedance θ_{JA} (see Note 3): D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the $\overline{SH/LD}$ input in conjunction with the CLK INH input.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | SN54165 | | | SN74165 | | | UNIT |
|----------------|--|---------|-----|------|---------|-----|------|---------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I_{OH} | High-level output current | | | -800 | | | -800 | μ A |
| I_{OL} | Low-level output current | | | 16 | | | 16 | mA |
| f_{clock} | Clock frequency | 0 | | 20 | 0 | | 20 | MHz |
| $t_{w(clock)}$ | Width of clock input pulse | 25 | | | 25 | | | ns |
| $t_{w(load)}$ | Width of load input pulse | 15 | | | 15 | | | ns |
| t_{su} | Clock-enable setup time (see Figure 1) | 30 | | | 30 | | | ns |
| t_{su} | Parallel input setup time (see Figure 1) | 10 | | | 10 | | | ns |
| t_{su} | Serial input setup time (see Figure 1) | 20 | | | 20 | | | ns |
| t_{su} | Shift setup time (see Figure 1) | 45 | | | 45 | | | ns |
| t_h | Hold time at any input | 0 | | | 0 | | | ns |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54165 | | | SN74165 | | | UNIT |
|---|--|---------|------|------|---------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| V _{IK} Input clamp voltage | V _{CC} = MIN, I _I = -12 mA | | | -1.5 | | | -1.5 | V |
| V _{OH} High-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V _{OL} Low-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I _I Input current at maximum input voltage | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA |
| I _{IH} High-level input current | SH/LD | | | 80 | | | 80 | µA |
| | Other inputs | | | 40 | | | 40 | |
| I _{IL} Low-level input current | SH/LD | | | -3.2 | | | -3.2 | mA |
| | Other inputs | | | -1.6 | | | -1.6 | |
| I _{OS} Short-circuit output current§ | V _{CC} = MAX | -20 | | -55 | -18 | | -55 | mA |
| I _{CC} Supply current | V _{CC} = MAX, See Note 4 | | 42 | 63 | | 42 | 63 | mA |

NOTE 4: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/LD, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

SN54165 and SN74165 switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------|----------------|--|-----|-----|-----|------|
| f _{max} | | | | 20 | 26 | | MHz |
| t _{PLH} | LD | Any | C _L = 15 pF, R _L = 400 Ω | | 21 | 31 | ns |
| t _{PHL} | | | | | 27 | 40 | |
| t _{PLH} | CLK | Any | C _L = 15 pF, R _L = 400 Ω | | 16 | 24 | ns |
| t _{PHL} | | | | | 21 | 31 | |
| t _{PLH} | H | Q _H | C _L = 15 pF, R _L = 400 Ω | | 11 | 17 | ns |
| t _{PHL} | | | | | 24 | 36 | |
| t _{PLH} | H | Q _H | C _L = 15 pF, R _L = 400 Ω | | 18 | 27 | ns |
| t _{PHL} | | | | | 18 | 27 | |

¶ f_{max} = maximum clock frequency, t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output



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recommended operating conditions

| | | SN54LS165A | | | SN74LS165A | | | UNIT | |
|-----------------------|---|------------|-----|------|------------|-----|------|------|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | |
| V _{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V | |
| I _{OH} | High-level output current | | | -0.4 | | | -0.4 | mA | |
| I _{OL} | Low-level output current | | | 4 | | | 8 | mA | |
| f _{clock} | Clock frequency | 0 | | 25 | 0 | | 25 | MHz | |
| t _{w(clock)} | Width of clock input pulse (see Figure 2) | Clock high | | 15 | | | 15 | ns | |
| | | Clock low | | 25 | | | 25 | | |
| t _{w(load)} | Width of load input pulse | Clock high | | 25 | | | 25 | ns | |
| | | Clock low | | 17 | | | 17 | | |
| t _{su} | Clock-enable setup time (see Figure 2) | | | 30 | | | 30 | ns | |
| t _{su} | Parallel input setup time (see Figure 2) | | | 10 | | | 10 | ns | |
| t _{su} | Serial input setup time (see Figure 2) | | | 20 | | | 20 | ns | |
| t _{su} | Shift setup time (see Figure 2) | | | 45 | | | 45 | ns | |
| t _h | Hold time at any input | | | 0 | | | 0 | ns | |
| T _A | Operating free-air temperature | | | -55 | | 125 | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITION† | SN54LS165A | | | SN74LS165A | | | UNIT | |
|-------------------|--|------------------------|------|------|------------|------|------|------|---|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | | | -1.5 | | | -1.5 | V | |
| V _{OH} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA | 2.5 | 3.5 | | 2.7 | 3.5 | | V | |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX | I _{OL} = 4 mA | | 0.25 | 0.4 | 0.25 | | 0.4 | V |
| | | I _{OL} = 8 mA | | | | 0.35 | | 0.5 | |
| I _I | V _{CC} = MAX, V _I = 7 V | | | 0.1 | | | 0.1 | mA | |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | 20 | | | 20 | μA | |
| I _{IL} | V _{CC} = MAX, V _I = 0.4 V | | | -0.4 | | | -0.4 | mA | |
| I _{OS} § | V _{CC} = MAX | -20 | | -100 | -20 | | -100 | mA | |
| I _{CC} | V _{CC} = MAX, See Note 4 | | 18 | 30 | | 18 | 30 | mA | |

NOTE 4. With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/LD, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.



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SN54LS165A and SN74LS165A switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

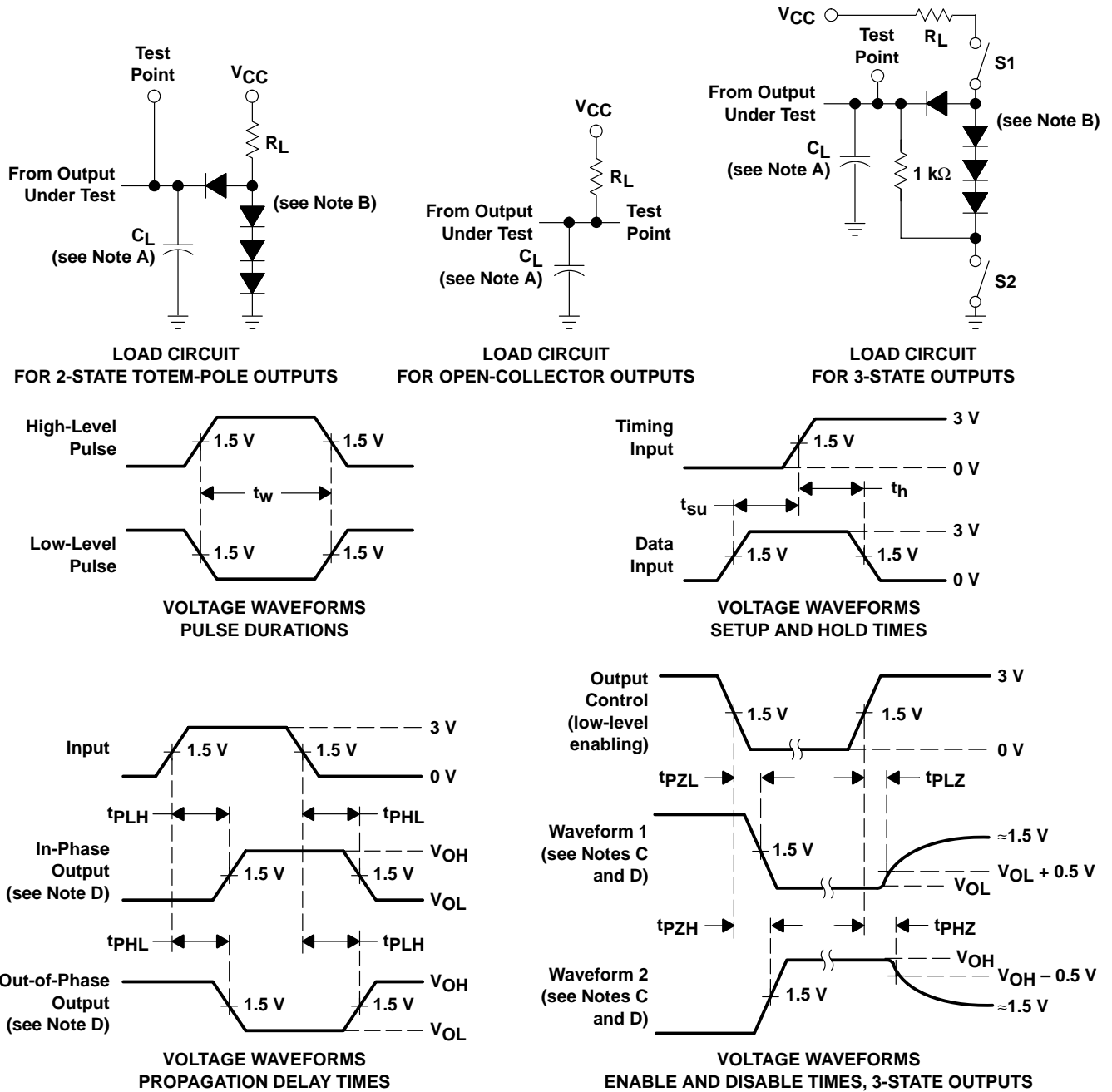
| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-----------------|------------------|---|-----|-----|-----|------|
| f_{max} | | | | 25 | 35 | | MHz |
| t_{PLH} | \overline{LD} | Any | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 21 | 35 | ns |
| t_{PHL} | | | | | 26 | 35 | |
| t_{PLH} | CLK | Any | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 14 | 25 | ns |
| t_{PHL} | | | | | 16 | 25 | |
| t_{PLH} | H | Q_H | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 13 | 25 | ns |
| t_{PHL} | | | | | 24 | 30 | |
| t_{PLH} | H | \overline{Q}_H | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 19 | 30 | ns |
| t_{PHL} | | | | | 17 | 25 | |

† f_{max} = maximum clock frequency, t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output



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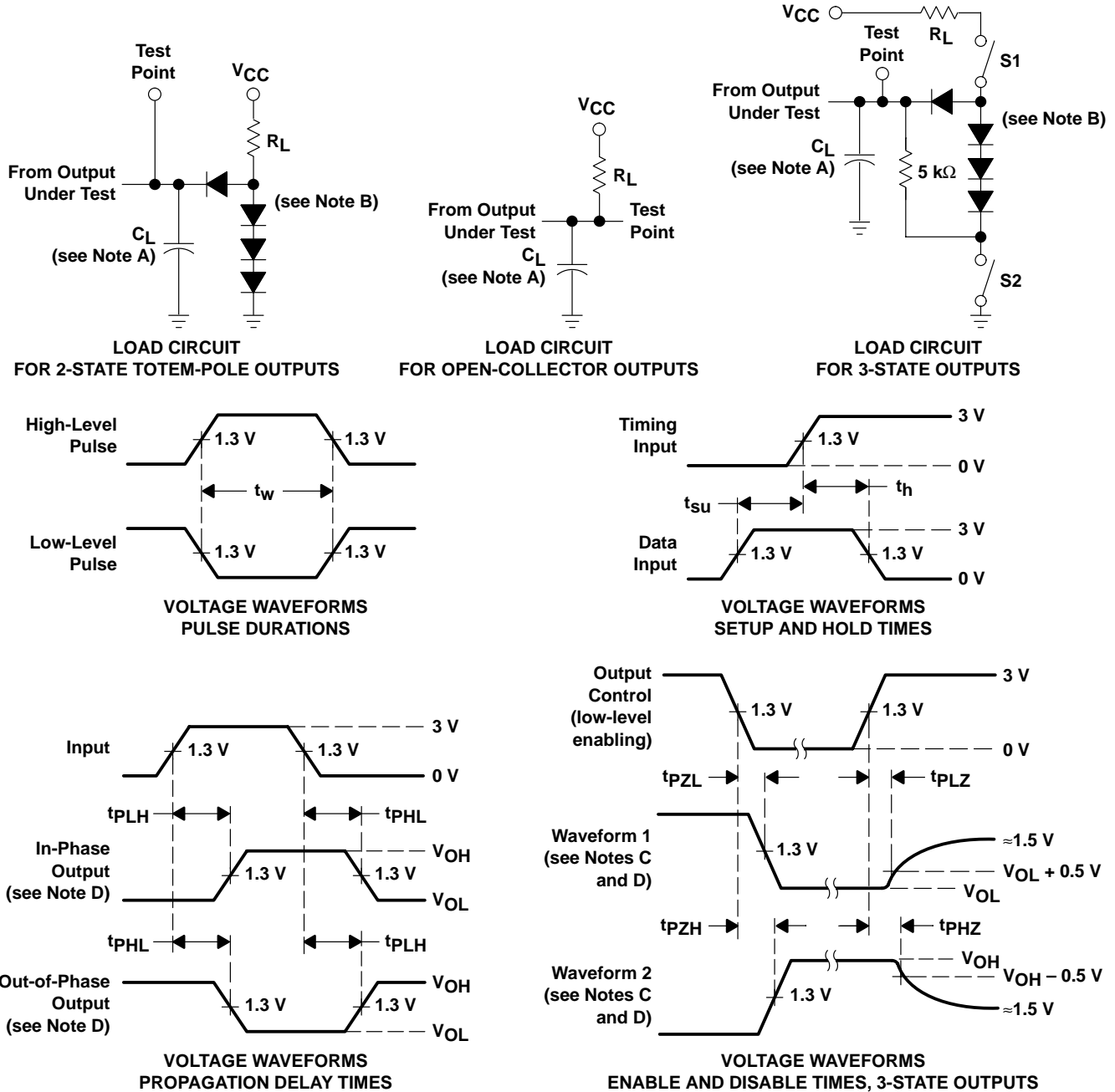
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 - F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-7700601VEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7700601VE A SNV54LS165AJ | Samples |
| 5962-7700601VFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7700601VF A SNV54LS165AW | Samples |
| 7700601EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7700601EA SNJ54LS165AJ | Samples |
| 7700601FA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7700601FA SNJ54LS165AW | Samples |
| JM38510/30608B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608B2A | Samples |
| JM38510/30608BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608BEA | Samples |
| JM38510/30608BFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608BFA | Samples |
| M38510/30608B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608B2A | Samples |
| M38510/30608BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608BEA | Samples |
| M38510/30608BFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 30608BFA | Samples |
| SN54LS165AJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS165AJ | Samples |
| SN74LS165AD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS165A | Samples |
| SN74LS165ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS165A | Samples |
| SN74LS165AN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS165AN | Samples |
| SN74LS165ANE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS165AN | Samples |
| SN74LS165ANSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS165A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------|-------------------------|
| SNJ54LS165AFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS165AFK | Samples |
| SNJ54LS165AJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7700601EA SNJ54LS165AJ | Samples |
| SNJ54LS165AW | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7700601FA SNJ54LS165AW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS165A, SN54LS165A-SP, SN74LS165A :

- Catalog : [SN74LS165A](#), [SN54LS165A](#)
- Military : [SN54LS165A](#)
- Space : [SN54LS165A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS165ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS165ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS165ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LS165ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-7700601VFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| 7700601FA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/30608B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/30608BFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/30608B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/30608BFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74LS165AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LS165AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS165AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS165ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS165ANE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS165AFK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS165AW | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

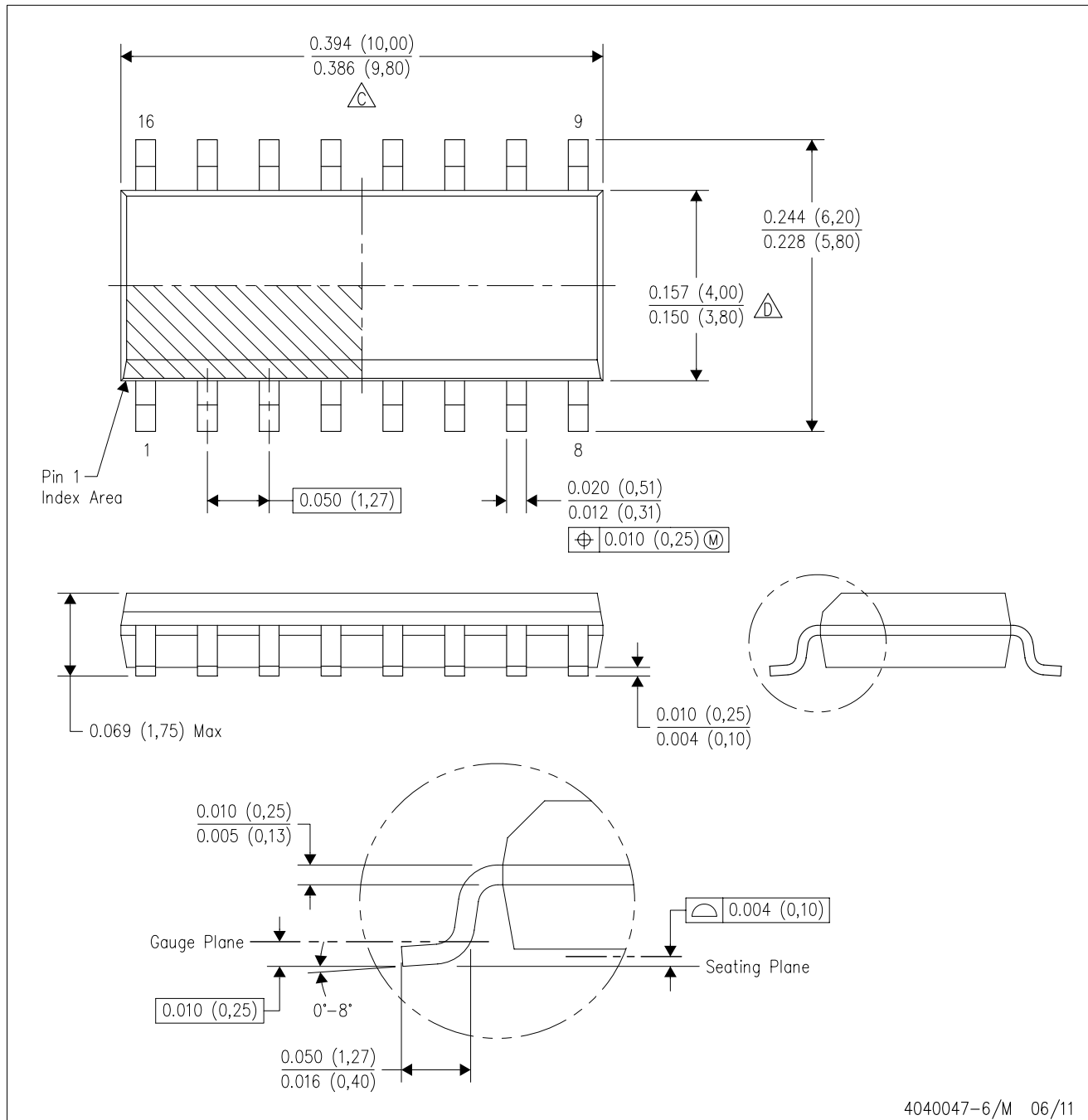


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

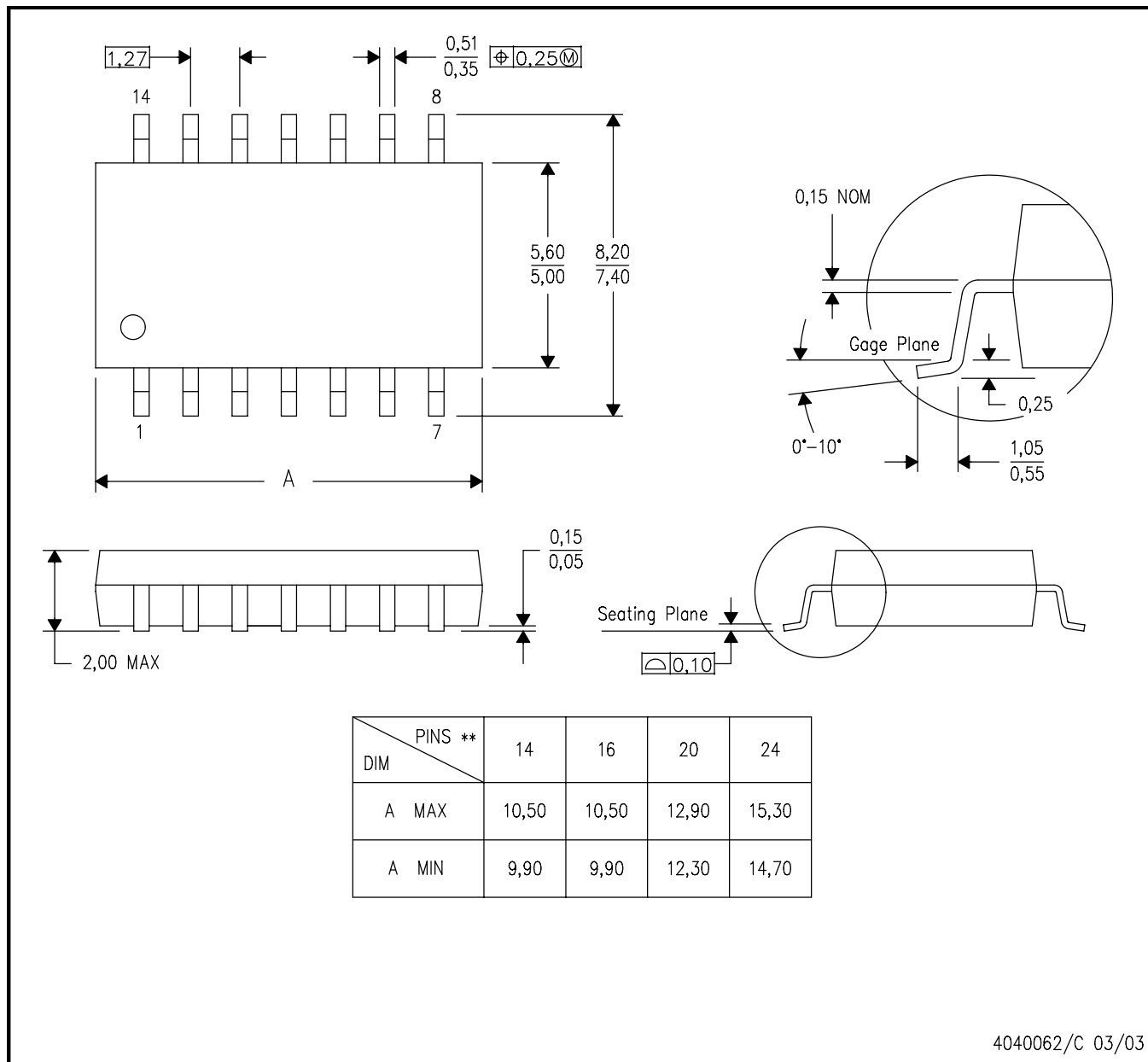
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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